14-Bit, 175 MSPS TxDAC® D/A Converter

Preliminary Technical Data

AD9707

FEATURES[1]

Low Power Member of Pin Compatible TxDAC Product Family
Power Dissipation @ 3.3 V:
- **21 mW @ 10 MSPS**
- **24 mW @ 25 MSPS**
- **30 mW @ 50 MSPS**

Sleep Mode: 5 mW @ 3.3 V
Supply Voltage: 1.7 V to 3.6 V
SFDR to Nyquist:
- **85 dBc @ 5 MHz Output**
- **80 dBc @ 10 MHz Output**
- **75 dBc @ 20 MHz Output**

SNR @ 10 MHz Output, 125 MSPS: TBD dB
Differential Current Outputs: 1 mA to 5 mA
Data Format: Twos Complement or Straight Binary
On-Chip 1.0 V Reference
CMOS Compatible Digital Interface
Edge-Triggered Latches

32-LEAD LFCSP PACKAGE FEATURES

Clock Input: Single-Ended and Differential
Output Common Mode: Adjustable 0 V to 1.2 V
Power-Down Mode: < 400 µW @ 3.3 V (SPI Controllable)
Serial Peripheral Interface (SPI)
Self-calibration
32-Lead LFCSP Pb-Free Package

28-LEAD TSSOP PACKAGE FEATURES

Internal 500Ω Load Resistor
Internal 16kΩ Resistor to Set Full Scale Current Output
Clock Input: Single-Ended
28-Lead TSSOP Pb-Free Package

[1] Protected by U.S. Patent Numbers 5568145, 5689257, and 5703519

FUNCTIONAL BLOCK DIAGRAMS

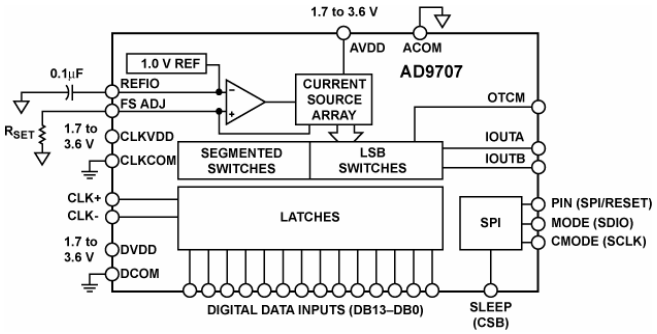

Figure 1. Functional Block Diagram (LFCSP Package)

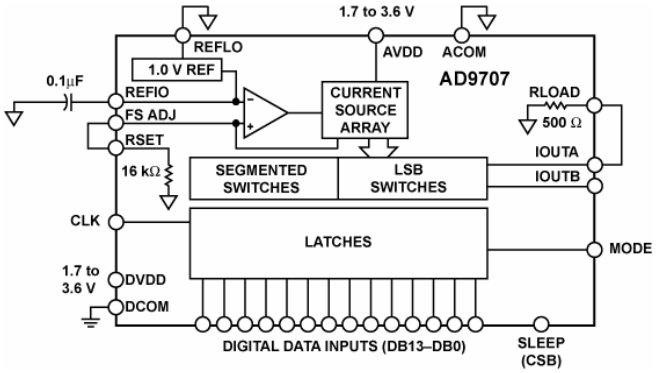

Figure 2. Functional Block Diagram (TSSOP Package)

Rev. PrB

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GENERAL DESCRIPTION

The AD9707 is a14-bit resolution, low power, fourth generation member of the TxDAC series of high performance, CMOS digital-to-analog converters (DACs). The AD970x family, consisting of 8-, 10-, 12-, and 14-bit DACs, is pin compatible with the AD974x family of TxDACs and is specifically optimized for the transmit signal path of communication systems. All of the devices share the same interface, small outline package, and pinout, providing an upward or downward component selection path based on performance, resolution, and cost. The AD9707 offers exceptional ac and dc performance while supporting update rates up to 175 MSPS.

The AD9707's flexible power supply operating range of 1.7 V to 3.6 V and low power dissipation makes it well suited for portable and low power applications. Its power dissipation can be further reduced to 15 mW with a slight degradation in performance by lowering the full-scale current output. Also, a power-down mode reduces the standby power dissipation to approximately 5 mW.

The AD9707-LFCSP has an optional serial peripheral interface (SPI) which provides a higher level of programmability to enhance performance of the DAC. An adjustable output common mode feature has also been added to the AD9707-LFCSP that allows for easy interfacing to other components that require common modes greater than 0 V.

Edge-triggered input latches and a 1.0 V temperature compensated band gap reference have been integrated to provide a complete monolithic DAC solution. The digital inputs support 1.8 V and 3.3 V CMOS logic families.

PRODUCT HIGHLIGHTS

1. Pin Compatible: The AD970x line of TxDACs is pin compatible with the AD974x TxDAC line.
2. Low power: Complete CMOS DAC operates on a single supply of 3.6 V down to 1.7 V, consuming 25mW (3.3V) and 10mW (1.8 V). The DAC full-scale current can be reduced for lower power operation, and sleep and power-down modes are provided for low power idle periods.
3. Self-Calibration (foreground) enables true 14-bit INL and DNL performance. (LFCSP only)
4. Data input supports twos complement or straight binary data coding.
5. High speed, single-ended and differential (LFCSP only) CMOS clock input supports 175 MSPS conversion rate.
6. SPI control offers higher level of programmability. (LFCSP package only)
7. Adjustable output common mode from 0 V to 1.2 V allows for easy interfacing to other components that accept common mode levels greater than 0 V (LFCSP only).
8. On-chip voltage reference: The AD9707 includes a 1.0 V temperature compensated band gap voltage reference.
9. Industry-standard 28-lead TSSOP and 32-lead LFCSP packages.

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AD9707–SPECIFICATIONS

DC SPECIFICATIONS (3.3 V)

(T_{MIN} to T_{MAX}, AVDD = 3.3 V, DVDD = 3.3 V, CLKVDD = 3.3 V, I_{OUTFS} = 2 mA, unless otherwise noted.)

Table 1.

Parameter	Min	Typ	Max	Unit
RESOLUTION	14			Bits
DC ACCURACY[1]				
Integral Nonlinearity (INL) Pre-calibration		± 3		LSB
Integral Nonlinearity (INL) Post-calibration[2]		± 0.8		LSB
Differential Nonlinearity (DNL) Pre-calibration		± 1.5		LSB
Differential Nonlinearity (DNL) Post-calibration[2]		± 0.7		LSB
ANALOG OUTPUT				
Offset Error	-0.02		+0.02	% of FSR
Gain Error (Without Internal Reference)				% of FSR
Gain Error (With Internal Reference)	-0.8	-0.2	+0.2	% of FSR
Full-Scale Output Current[3]	1	2	5	mA
Output Compliance Range	-1		+1.25	V
Output Resistance		200		MΩ
Output Capacitance		5		pF
REFERENCE OUTPUT				
Reference Voltage		1.0		V
Reference Output Current[4]		100		nA
REFERENCE INPUT				
Input Compliance Range	0.1		1.25	V
Reference Input Resistance (Ext. Reference)		1		MΩ
Small Signal Bandwidth		0.5		MHz
TEMPERATURE COEFFICIENTS				
Offset Drift		0		ppm of FSR/°C
Gain Drift (Without Internal Reference)		TBD		ppm of FSR/°C
Gain Drift (With Internal Reference)		± 70		ppm of FSR/°C
Reference Voltage Drift		± 80		ppm/°C
POWER SUPPLY				
Supply Voltages				
AVDD	2.5	3.3	3.6	V
DVDD	2.5	3.3	3.6	V
CLKVDD	2.5	3.3	3.6	V
Analog Supply Current (I_{AVDD})		4.5		mA
Digital Supply Current (I_{DVDD})[5]		1.1		mA
Clock Supply Current (I_{CLKVDD})		1.7		mA
Supply Current Sleep Mode (I_{AVDD})		0.4	1.0	mA
Supply Current Power-Down Mode		20		µA
Power Dissipation[5]		24		mW
Power Supply Rejection Ratio—AVDD[6]	-1		+1	% of FSR/V
Power Supply Rejection Ratio—DVDD	-0.04		+0.04	% of FSR/V
OPERATING RANGE	-40		+85	°C

[1] Measured at IOUTA, driving a virtual ground.
[2] Calibration offered in LFCSP package only.
[3] Nominal full-scale current, I_{OUTFS}, is 32 times the I_{REF} current.
[4] An external buffer amplifier with input bias current <100 nA should be used to drive any external load.
[5] Measured at f_{CLOCK} = 25 MSPS and f_{OUT} = 2.5 MHz.
[6] ±5% power supply variation.

DYNAMIC SPECIFICATIONS (3.3V)

(T_{MIN} to T_{MAX} , AVDD = 3.3 V, DVDD = 3.3 V, CLKVDD = 3.3 V, I_{OUTFS} = 2 mA, differential transformer coupled output, 500 Ω terminated, unless otherwise noted.)

Table 2

Parameter	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE				
Maximum Output Update Rate (f_{CLOCK})	175			MSPS
Output Settling Time (t_{ST}) (to 0.1%)[1]		TBD		ns
Output Propagation Delay (t_{PD})		TBD		ns
Glitch Impulse		TBD		pV-s
Output Rise Time (10% to 90%)		TBD		ns
Output Fall Time (10% to 90%)		TBD		ns
Output Noise (I_{OUTFS} = 2 mA)[2]		45		pA/√Hz
Noise Spectral Density[2]		-150		dBc/Hz
AC LINEARITY				
Spurious-Free Dynamic Range to Nyquist				
f_{CLOCK} = 10 MSPS; f_{OUT} = 1.00 MHz		82		dBc
f_{CLOCK} = 25 MSPS; f_{OUT} = 1.00 MHz		80		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 5.00 MHz		80		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 10 MHz		80		dBc
f_{CLOCK} = 125 MSPS; f_{OUT} = 15 MHz		80		dBc
f_{CLOCK} = 125 MSPS; f_{OUT} = 25 MHz		79		dBc
f_{CLOCK} = 175 MSPS; f_{OUT} = 20 MHz		78		dBc
f_{CLOCK} = 175 MSPS; f_{OUT} = 40 MHz		75		dBc
Total Harmonic Distortion				
f_{CLOCK} = 25 MSPS; f_{OUT} = 1.00 MHz		-78		dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 2.00 MHz		-78		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 2.00 MHz		-78		dBc
f_{CLOCK} = 125 MSPS; f_{OUT} = 2.00 MHz		-78		dBc
Signal-to-Noise Ratio				
f_{CLOCK} = 65 MSPS; f_{OUT} = 5 MHz; I_{OUTFS} = 2 mA		82		dB
f_{CLOCK} = 125 MSPS; f_{OUT} = 5 MHz; I_{OUTFS} = 2 mA		77		dB
f_{CLOCK} = 175 MSPS; f_{OUT} = 5 MHz; I_{OUTFS} = 2 mA		70		dB
Multitone Power Ratio (8 Tones at 400 kHz Spacing)				
f_{CLOCK} = 78 MSPS; f_{OUT} = 15.0 MHz to 18.2 MHz				
0 dBFS Output		TBD		dBc
- 6 Dbfs Output		TBD		dBc
-12 dBFS Output		TBD		dBc
-18 dBFS Output		TBD		dBc

[1] Measured single-ended into 500 Ω•load.
[2] Noise spectral density is the average noise power normalized to a 1 Hz bandwidth, with the DAC converting and producing an output tone. Measured single-ended into a 500 Ω load.

DIGITAL SPECIFICATIONS (3.3V)

(T_{MIN} to T_{MAX} , AVDD = 3.3 V, DVDD = 3.3 V, CLKVDD = 3.3 V, I_{OUTFS} = 2 mA, unless otherwise noted.)

Table 3

Parameter	Min	Typ	Max	Unit
DIGITAL INPUTS[1]				
Logic 1 Voltage	2.1	3		V
Logic 0 Voltage		0	0.9	V
Logic 1 Current	-10		+10	µA
Logic 0 Current			+10	µA
Input Capacitance		5		pF
Input Setup Time (t_S)		TBD		ns
Input Hold Time (t_H)		TBD		ns
Latch Pulsewidth (t_{LPW})		TBD		ns
CLK INPUTS[2]				
Input Voltage Range	0		3	V
Common-Mode Voltage	0.75	1.5	2.25	V
Differential Voltage	0.5	1.5		V

[1] Includes CLOCK pin on TSSOP packages and CLK+ pin on LFCSP package in single-ended clock input mode.
[2] Applicable to CLK+ and CLK– inputs when configured for differential clock input mode.

DC SPECIFICATIONS (1.8V)

(T_{MIN} to T_{MAX}, AVDD = 1.8 V, DVDD = 1.8 V, CLKVDD = 1.8 V, I_{OUTFS} = 1 mA, unless otherwise noted.)

Table 4.

Parameter	Min	Typ	Max	Unit
RESOLUTION	14			Bits
DC ACCURACY[1]				
Integral Nonlinearity (INL) Pre-calibration		± 3		LSB
Integral Nonlinearity (INL) Post-calibration[2]		± 0.8		LSB
Differential Nonlinearity (DNL) Pre-calibration		± 1.5		LSB
Differential Nonlinearity (DNL) Post-calibration[2]		± 0.5		LSB
ANALOG OUTPUT				
Offset Error	-0.02		+0.02	% of FSR
Gain Error (Without Internal Reference)				% of FSR
Gain Error (With Internal Reference)	-0.5	± 0.1	+0.5	% of FSR
Full-Scale Output Current[3]		1		mA
Output Compliance Range	-0.5		+0.6	V
Output Resistance		200		MΩ
Output Capacitance		5		pF
REFERENCE OUTPUT				
Reference Voltage		1.0		V
Reference Output Current[4]		100		nA
REFERENCE INPUT				
Input Compliance Range	0.1		1.25	V
Reference Input Resistance (Ext. Reference)		1		MΩ
Small Signal Bandwidth		0.5		MHz
TEMPERATURE COEFFICIENTS				
Offset Drift		0		ppm of FSR/°C
Gain Drift (Without Internal Reference)				ppm of FSR/°C
Gain Drift (With Internal Reference)		± 70		ppm of FSR/°C
Reference Voltage Drift		± 80		ppm/°C
POWER SUPPLY				
Supply Voltages				
AVDD	1.7	1.8		V
DVDD	1.7	1.8		V
CLKVDD	1.7	1.8		V
Analog Supply Current (I_{AVDD})		3.1		mA
Digital Supply Current (I_{DVDD})[5]		0.5		mA
Clock Supply Current (I_{CLKVDD})		0.7		mA
Supply Current Sleep Mode (I_{AVDD})		0.3		mA
Supply Current Power-Down Mode		18		µA
Power Dissipation[5]		8		mW
Power Supply Rejection Ratio—AVDD[6]	-1		+1	% of FSR/V
Power Supply Rejection Ratio—DVDD	-0.04		+0.04	% of FSR/V
OPERATING RANGE	-40		+85	°C

[1] Measured at IOUTA, driving a virtual ground.
[2] Calibration offered in LFCSP package only.
[3] Nominal full-scale current, I_{OUTFS}, is 32 times the I_{REF} current.
[4] An external buffer amplifier with input bias current <100 nA should be used to drive any external load.
[5] Measured at f_{CLOCK} = 25 MSPS and f_{OUT} = 1 MHz.
[6] ±5% power supply variation.

DYNAMIC SPECIFICATIONS (1.8V)

(T_{MIN} to T_{MAX} , AVDD = 1.8 V, DVDD = 1.8 V, CLKVDD = 1.8 V, I_{OUTFS} = 1 mA, differential transformer coupled output, 500 Ω doubly terminated, unless otherwise noted.)

Table 5

Parameter	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE				
Maximum Output Update Rate (f_{CLOCK})	80			MSPS
Output Settling Time (t_{ST}) (to 0.1%)[1]		TBD		ns
Output Propagation Delay (t_{PD})		TBD		ns
Glitch Impulse		TBD		pV-s
Output Rise Time (10% to 90%)		TBD		ns
Output Fall Time (10% to 90%)		TBD		ns
Output Noise (I_{OUTFS} = 2 mA)[2]		45		pA/√Hz
Noise Spectral Density[2]		-150		dBc/Hz
AC LINEARITY				
Spurious-Free Dynamic Range to Nyquist				
f_{CLOCK} = 10 MSPS; f_{OUT} = 1.00 MHz		79		
f_{CLOCK} = 25 MSPS; f_{OUT} = 1.00 MHz		78		dBc
f_{CLOCK} = 25 MSPS; f_{OUT} = 5 MHz		77		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 10 MHz		76		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 15 MHz		73		dBc
f_{CLOCK} = 80 MSPS; f_{OUT} = 15 MHz		71		dBc
f_{CLOCK} = 80 MSPS; f_{OUT} = 30 MHz		63		dBc
Total Harmonic Distortion				
f_{CLOCK} = 10 MSPS; f_{OUT} = 1.00 MHz		-79		dBc
f_{CLOCK} = 25 MSPS; f_{OUT} = 2.00 MHz		-75		dBc
f_{CLOCK} = 45 MSPS; f_{OUT} = 2.00 MHz		-75		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 2.00 MHz		-75		dBc
Signal-to-Noise Ratio				
f_{CLOCK} = 25 MSPS; f_{OUT} = 5 MHz; I_{OUTFS} = 1 mA		76		dB
f_{CLOCK} = 45 MSPS; f_{OUT} = 5 MHz; I_{OUTFS} = 1 mA		74		dB
f_{CLOCK} = 65 MSPS; f_{OUT} = 5 MHz; I_{OUTFS} = 1 mA		70		dB
Multitone Power Ratio (8 Tones at 400 kHz Spacing)				
f_{CLOCK} = 40 MSPS; f_{OUT} = 10 MHz to 13.2 MHz				
0 dBFS Output		TBD		dBc
- 6 dBFS Output		TBD		dBc
-12 dBFS Output		TBD		dBc
-18 dBFS Output		TBD		dBc

[1] Measured single-ended into 500 Ω•load.
[2] Noise spectral density is the average noise power normalized to a 1 Hz bandwidth, with the DAC converting and producing an output tone. Measured single-ended into 500 Ω load.

DIGITAL SPECIFICATIONS (1.8V)

(T_{MIN} to T_{MAX} , AVDD = 1.8 V, DVDD = 1.8 V, CLKVDD = 1.8 V, I_{OUTFS} = 1 mA, unless otherwise noted.)

Table 6

Parameter	Min	Typ	Max	Unit
DIGITAL INPUTS[1]				
Logic 1 Voltage	1.2	1.8		V
Logic 0 Voltage		0	0.5	V
Logic 1 Current	-10		+10	µA
Logic 0 Current			+10	µA
Input Capacitance		5		pF
Input Setup Time (t_S)		TBD		ns
Input Hold Time (t_H)		TBD		ns
Latch Pulsewidth (t_{LPW})		TBD		ns
CLK INPUTS[2]				
Input Voltage Range	0		1.8	V
Common-Mode Voltage	0.4	0.9	1.3	V
Differential Voltage	0.5	1.5		V

[1] Includes CLOCK pin on TSSOP packages and CLK+ pin on LFCSP package in single-ended clock input mode.
[2] Applicable to CLK+ and CLK– inputs when configured for differential clock input mode.

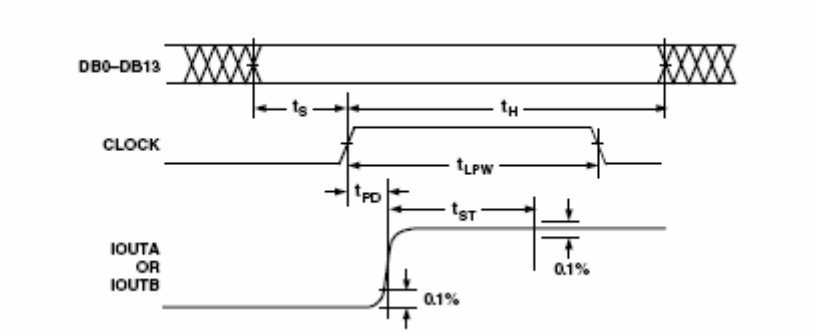


Figure 3. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	With Respect to	Min	Max	Unit
AVDD	ACOM	-0.3	+3.9	V
DVDD	DCOM	-0.3	+3.9	V
CLKVDD	CLKCOM	-0.3	+3.9	V
ACOM	DCOM	-0.3	+0.3	V
ACOM	CLKCOM	-0.3	+0.3	V
DCOM	CLKCOM	-0.3	+0.3	V
AVDD	DVDD	-3.9	+3.9	V
AVDD	CLKVDD	-3.9	+3.9	V
DVDD	CLKVDD	-3.9	+3.9	V
CLOCK, SLEEP	DCOM	-0.3	DVDD+0.3	V
Digital Inputs, MODE	DCOM	-0.3	DVDD+0.3	V
IOUTA, IOUTB	ACOM	-1.0	AVDD+0.3	V
REFIO, REFLO, FS ADJ	ACOM	-0.3	AVDD+0.3	V
CLK+, CLK–, CMODE	CLKCOM	-0.3	CLKVDD+0.3	V
Junction Temperature			150	°C
Storage Temperature		-65	+150	°C
Lead Temperature (10 sec)			300	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

THERMAL CHARACTERISTICS[1]

Thermal Resistance

28-Lead TSSOP

θ_{JA} = 67.7°C/W

32-Lead LFCSP

θ_{JA} = 32.5°C/W

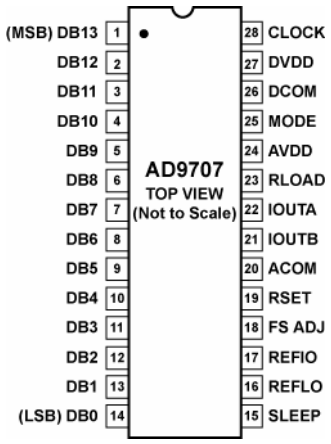
[1] Thermal impedance measurements were taken on a 4-layer board in still air, in accordance with EIA/JESD51-7.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

28-Lead TSSOP



32-Lead LFCSP

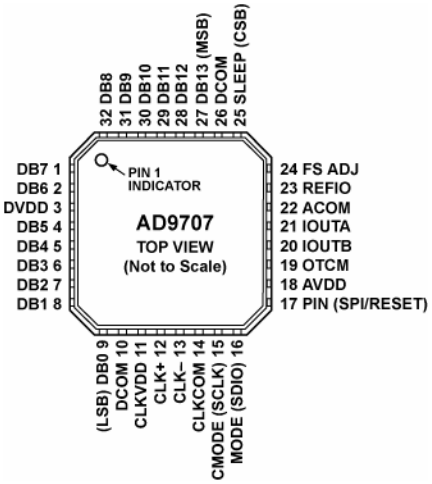


Figure 4. Pin Configurations (TSSOP and LFCSP packages)

Table 8. Pin Function Descriptions

TSSOP Pin No.	LFCSP Pin No.	Mnemonic	Description
1	27	DB13	Most Significant Data Bit (MSB).
2–13	28–32, 1, 2, 4–8	DB12–DB1	Data Bits 12–1.
14	9	DB0	Least Significant Data Bit (LSB).
15	25	SLEEP / CSB	Power-Down Control Input. Active high. Contains active pull-down circuit; it may be left unterminated if not used. Must be driven low during SPI operation.
16	N/A	REFLO	Reference Ground when Internal 1.0 V Reference Used. Connect to AVDD to disable internal reference.
17	23	REFIO	Reference Input/Output. Serves as reference input when internal reference disabled. Serves as 1.0 V reference output when internal reference activated. Requires 0.1 µF capacitor to ACOM when internal reference activated.
18	24	FS ADJ	Full-Scale Current Output Adjust.
19	N/A	RSET	Internal 16K Resistor. Connect to pin 18 (FSADJ) to set 2 mA Full-Scale Output Current; it may be left floating if not used. Refer to page 21 for details.
20	22	ACOM	Analog Common.
21	20	IOUTB	Complementary DAC Current Output. Full-scale current when all data bits are 0s.
22	21	IOUTA	DAC Current Output. Full-scale current when all data bits are 1s.
23	N/A	RLOAD	Internal 500Ω Termination Resistor. Refer to page 21 for details.
24	18	AVDD	Analog Supply Voltage (1.7 V – 3.6 V).
N/A	19	OTCM	Adjustable Output Common Mode. Refer to page 21 for details.
N/A	17	PIN / SPI/RESET	Selects SPI mode or Pin mode operation. Active low for SPI operation. Active high for non-SPI operation. Pulse high to reset SPI registers to default values.
25	16	MODE / SDIO	Selects Input Data Format. Connect to DCOM for straight binary, DVDD for twos complement. When SPI is enabled (LFCSP package only), this pin acts as SPI data input / output.
N/A	15	CMODE / SCLK	Clock Mode Selection. Connect to CLKCOM for single-ended clock receiver (drive CLK+ and float CLK–). Connect to CLKVDD for differential receiver. When SPI is enabled, SPI data clock input.
26	10, 26	DCOM	Digital Common.
27	3	DVDD	Digital Supply Voltage (1.7 V – 3.6 V)
28	N/A	CLOCK	Clock Input. Data latched on positive edge of clock.
N/A	12	CLK+	Differential Clock Input.
N/A	13	CLK–	Differential Clock Input.
N/A	11	CLKVDD	Clock Supply Voltage (1.7 V – 3.6 V).
N/A	14	CLKCOM	Clock Common.

DEFINITIONS OF SPECIFICATIONS

Linearity Error (Also Called Integral Nonlinearity or INL)

Linearity error is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (or DNL)

DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity

A D/A converter is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error

The deviation of the output current from the ideal of zero is called the offset error. For IOUTA, 0 mA output is expected when the inputs are all 0s. For IOUTB, 0 mA output is expected when all inputs are set to 1s.

Gain Error

The difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1s minus the output when all inputs are set to 0s.

Output Compliance Range

The range of allowable voltage at the output of a current output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift

Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per °C. For reference drift, the drift is reported in ppm per °C.

Power Supply Rejection

The maximum change in the full-scale output as the supplies are varied from nominal to minimum and maximum specified voltages.

Settling Time

The time required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition.

Glitch Impulse

Asymmetrical switching times in a DAC give rise to undesired output transients that are quantified by a glitch impulse. It is specified as the net area of the glitch in pV-s.

Spurious-Free Dynamic Range

The difference, in dB, between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal. It is expressed as a percentage or in decibels (dB).

Multitone Power Ratio

The spurious-free dynamic range containing multiple carrier tones of equal amplitude. It is measured as the difference between the rms amplitude of a carrier tone to the peak spurious signal in the region of a removed tone.

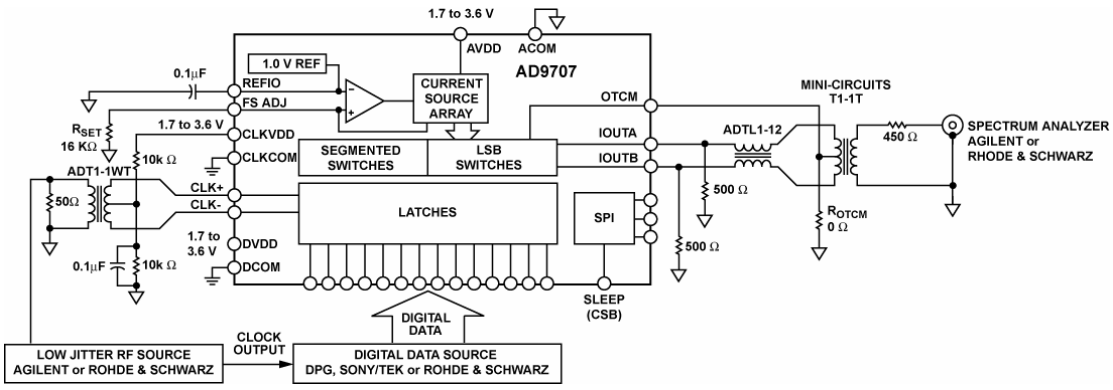


Figure 5. Basic AC Characterization Test Set-Up (LFCSP Package)

AD9707–TYPICAL PERFORMANCE CHARACTERISTICS

TBD

Figure 6. SFDR vs. f_{OUT}

TBD

Figure 7. SFDR vs. f_{OUT} @ 25 MSPS

TBD

Figure 8. SFDR vs. f_{OUT} @ 125 MSPS

TBD

Figure 9. SFDR vs. f_{OUT} @ 175 MSPS

TBD

Figure 10. SFDR vs. f_{OUT} and I_{OUTFS} @ 65 MSPS

TBD

Figure 11. Single-Tone SFDR vs. A_{OUT} @ $f_{OUT}=f_{CLOCK}/11$

TBD

Figure 12. Single-Tone SFDR vs. A_{OUT} @ $f_{OUT}=f_{CLOCK}/5$

TBD

Figure 13. SNR vs. f_{CLOCK} and I_{OUTFS} @ f_{OUT}=5 MHz and 0 dBFS

TBD

Figure 14. Dual-Tone IMD vs. A_{OUT} @ $f_{OUT}=f_{CLOCK}/7$

TBD

Figure 15. Typical INL

TBD

Figure 16. Typical DNL

TBD

Figure 17. SFDR vs. Temperature @ 125 MSPS

TBD

Figure 18. Single-Tone SFDR

TBD

Figure 19. Dual-Tone SFDR

TBD

Figure 20. Four-Tone SFDR

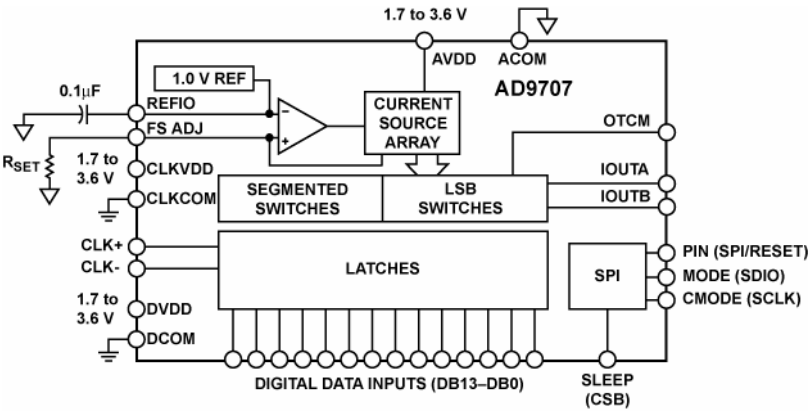


Figure 21. Simplified Block Diagram (LFCSP Package)

FUNCTIONAL DESCRIPTION

Figure 21 shows a simplified block diagram of the AD9707. The AD9707 consists of a DAC, digital control logic, and full-scale output current control. The DAC contains a PMOS current source array capable of providing a nominal full-scale current (I_{OUTFS}) of 2 mA and a maximum of 5 mA. The array is divided into 31 equal currents that make up the five most significant bits (MSBs). The next four bits, or middle bits, consist of 15 equal current sources whose value is 1/16th of an MSB current source. The remaining LSBs are binary weighted fractions of the middle bits current sources. Implementing the middle and lower bits with current sources, instead of an R-2R ladder, enhances its dynamic performance for multitone or low amplitude signals and helps maintain the DAC's high output impedance (i.e., >200MΩ).

All of these current sources are switched to one or the other of the two output nodes (i.e., IOUTA or IOUTB) via PMOS differential current switches. The switches are based on the architecture that was pioneered in the AD9764 family, with further refinements to reduce distortion contributed by the switching transient. This switch architecture also reduces various timing errors and provides matching complementary drive signals to the inputs of the differential current switches.

The analog and digital sections of the AD9707 have separate power supply inputs (i.e., AVDD and DVDD) that can operate independently over a 1.7 V to 3.6 V range. The digital section, which is capable of operating at a rate of up to 175 MSPS, consists of edge-triggered latches and segment decoding logic circuitry. The analog section includes the PMOS current sources, the associated differential switches, a 1.0 V band gap voltage reference, and a reference control amplifier.

The DAC full-scale output current is regulated by the reference control amplifier and can be set from 1 mA to 5 mA via an external resistor, R_{SET}, connected to the full-scale adjust (FS ADJ) pin. The external resistor, in combination with both the reference control amplifier and voltage reference V_{REFIO}, sets the reference current I_{REF}, which is replicated to the segmented current sources with the proper scaling factor. The full-scale current, I_{OUTFS}, is 32 times I_{REF}.

The AD9707-LFCSP provides the option of setting the output common mode to a value other than ACOM via the output common mode (OTCM) pin. This option allows the user to directly interface the output of the AD9707 to components that require common mode levels greater than 0 V.

SERIAL PERIPHERAL INTERFACE (LFCSP ONLY)

The AD9707 serial port is a flexible, synchronous serial communications port allowing easy interface to many industry standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola SPI® and Intel® SSR protocols. The interface allows read/write access to all registers that configure the AD9707. Single or multiple byte transfers are supported, as well as MSB first or LSB first transfer formats. The AD9707's serial interface port is configured as a single pin I/O.

General Operation of the Serial Interface

There are two phases to a communication cycle with the AD9707. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9707, coincident with the first eight SCLK rising edges. The instruction byte provides the AD9707 serial port controller with information regarding the data transfer cycle, which is Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is read or write, the number of bytes in the data transfer, and the starting register address for the first byte of the data transfer. The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9707.

A logic high on pin 17 (SPI RES/PIN), followed by a logic low, will reset the SPI port timing to the initial state of the instruction cycle. This is true regardless of the present state of the internal registers or the other signal levels present at the inputs to the SPI port. If the SPI port is in the midst of an instruction cycle or a data transfer cycle, none of the present data will be written.

The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9707 and the system controller. Phase 2 of the communication cycle is a transfer of 1, 2, 3, or 4 data bytes as determined by the instruction byte. Using one multibyte transfer is the preferred method. Single byte data transfers are useful to reduce CPU overhead when register access requires one byte only. Registers change immediately upon writing to the last bit of each transfer byte.

Instruction Byte

The instruction byte contains the information shown in Table 9.

MSB							**LSB**
I7	I6	I5	I4	I3	I2	I1	I0
R/W	N1	N0	A4	A3	A2	A1	A0

Table 9. SPI Instruction Byte

R/W, Bit 7 of the instruction byte, determines whether a read or a write data transfer will occur after the instruction byte write. Logic high indicates read operation. Logic 0 indicates a write operation. N1, N0, Bits 6 and 5 of the instruction byte, determine the number of bytes to be transferred during the data transfer cycle. The bit decodes are shown in Table 10.

A4, A3, A2, A1, A0, Bits 4, 3, 2, 1, 0 of the instruction byte, determine which register is accessed during the data transfer portion of the communications cycle. For multibyte transfers, this address is the starting byte address. The remaining register addresses are generated by the AD9707 based on the DATADIR bit (REG00, bit 6).

N1	N1	Description
0	0	Transfer 1 Byte
0	1	Transfer 2 Bytes
1	0	Transfer 3 Bytes
1	1	Transfer 4 Bytes

Table 10. Byte Transfer Count

Serial Interface Port Pin Descriptions

SCLK—Serial Clock. The serial clock pin is used to synchronize data to and from the AD9707 and to run the internal state machines. SCLK's maximum frequency is 20 MHz. All data input to the AD9707 is registered on the rising edge of SCLK. All data is driven out of the AD9707 on the falling edge of SCLK.

CSB—Chip Select. Active low input starts and gates a communication cycle. It allows more than one device to be used on the same serial communications lines. The SDIO pin will go to a high impedance state when this input is high. Chip select should stay low during the entire communication cycle.

SDIO—Serial Data I/O. This pin is used as a bidirectional data line to transmit and receive data.

MSB/LSB Transfers

The AD9707 serial port can support both most significant bit (MSB) first or least significant bit (LSB) first data formats. This functionality is controlled by register bit DATADIR (REG00, bit 6). The default is MSB first (DATADIR = 0).

When DATADIR = 0 (MSB first) the instruction and data bytes must be written from most significant bit to least significant bit. Multibyte data transfers in MSB first format start with an instruction byte that includes the register address of the most significant data byte. Subsequent data bytes should follow in order from high address to low address. In MSB first mode, the serial port internal byte address generator decrements for each data byte of the multibyte communication cycle.

When DATADIR = 1 (LSB first) the instruction and data bytes must be written from least significant bit to most significant bit. Multibyte data transfers in LSB first format start with an instruction byte that includes the register address of the least significant data byte followed by multiple data bytes. The serial port internal byte address generator increments for each byte of the multibyte communication cycle.

The AD9707 serial port controller data address will decrement from the data address written toward 0x00 for multibyte I/O operations if the MSB first mode is active. The serial port controller address will increment from the data address written toward 0x1F for multibyte I/O operations if the LSB first mode is active.

Notes on Serial Port Operation

The AD9707 serial port configuration is controlled by REG00, bit 7. It is important to note that the configuration changes immediately upon writing to the last bit of the register. For multibyte transfers, writing to this register may occur during the middle of communication cycle. Care must be taken to compensate for this new configuration for the remaining bytes of the current communication cycle.

The same considerations apply to setting the software reset, RESET (REG00, bit 5). All registers are set to their default values EXCEPT REG00 which remains unchanged.

Use of only single byte transfers when changing serial port configurations or initiating a software reset is recommended to prevent unexpected device behavior.

TBD

Figure 22. Serial Register Interface Timing MSB First

TBD

Figure 23. Serial Register Interface Timing LSB First

TBD

Figure 24. Timing Diagram for SPI Register Write

TBD

Figure 25. Timing Diagram for SPI Register Read

SPI REGISTER MAP

Table 11

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPI CTL	00	SDIODIR	DATADIR	SWRST	LNGINS	PDN	SLEEP	CLKOFF	EXREF
DATA	02	DATAFMT			DCLKPOL	LOWSKEW	CLKDIFF		CALCLK
CALMEM	0E			CALMEM[1]	CALMEM[0]	DIVSEL[3]	DIVSEL[2]	DIVSEL[1]	DIVSEL[0]
MEMRDWR	0F	CALSTAT	CALEN			SMEMWR	SMEMRD		UNCAL
MEMADDR	10			MEMADDR[5]	MEMADDR[4]	MEMADDR[3]	MEMADDR[2]	MEMADDR[1]	MEMADDR[0]
MEMDATA	11			MEMDATA[5]	MEMDATA[4]	MEMDATA[3]	MEMDATA[2]	MEMDATA[1]	MEMDATA[0]
ANAETST	17					PRELDS1			

SPI REGISTER DESCRIPTIONS

Table 12

SPI CNTL (00)	Bit	Direction (I/O)	Default	Description
SDIODIR	7	I	1	1: SDIO pin hardwired for input or output during data transfer (3-wire interface)
DATADIR	6	I	0	0: Serial data uses MSB first format 1: Serial data uses LSB first format
SWRST	5	I	0	0: Software reset not enabled (running) 1: Default all serial register bits, except address 00h
LNGINS	4	I	0	0: Use 1 byte premable (5 address bits) 1: Use 2 byte preamble (13 adress bits)
PDN	3	I	0	1: All analog and digital circuitry off, except serial interface
SLEEP	2	I	0	1: DAC output current off
CLKOFF	1	I	0	1: Clock off
EXREF	0	I	0	0: Internal bandgap reference 1: External reference

DATA (02)	Bit	Direction (I/O)	Default	Description
DATAFMT	7	I	0	0: Unsigned binary input data format 1: 2's complement input data format
DCLKPOL	4	I	0	0: Data latched on DATACLK rising edge 1: Data latched on DATACLK falling edge
LOWSKEW	3	I	0	0: Low skew mode disabled 1: Low skew mode enabled
CLKDIFF	2	I	0	0: Single-ended clock input 1: Differential clock input
CALCLK	0	I	0	0: Calibration clock disabled 1: Calibration clock enabled

CALMEM (0E)	Bit	Direction (I/O)	Default	Description
CALMEM[5:4]	[5:4]	O	00	Calibration Memory 00: Uncalibrated 01: Self calibration 11: User input
DIVSEL[2:0]	[3:0]	I	0000	Calibration clock divide ratio from channel data rate 0000: / 256 0001: / 128 : 1110: / 2 1111: / 1

MEMRDWR (0F)	Bit	Direction (I/O)	Default	Description
CALSTAT	7	O	0	0: Calibration cycle not complete 1: Calibration cycle complete
CALEN	6	I	0	1: Calibration in progress
SMEMWR	3	I	0	1: Write static memory data from external port
SMEMRD	2	I	0	1: Read static memory to external port
UNCAL	0	I	0	1: Use uncalibrated

MEMADDR (10)	Bit	Direction (I/O)	Default	Description
MEMADDR[5:0]	[5:0]	I/O	00000	Address of static memory to be accessed

MEMDATA (11)	Bit	Direction (I/O)	Default	Description
MEMDATA[5:0]	[5:0]	I/O	11111	Data for static memory access

ANAETST (17)	Bit	Direction (I/O)	Default	Description
PRELDS1	3	I	0	0: Pre-load calibration reference specified by user 1: Pre-load calibration reference of 32

REFERENCE OPERATION

The AD9707 contains an internal 1.0 V band gap reference. The internal reference can be disabled in both packages. To disable the reference in the 32-lead LFCSP package, a logic 1 must be written to REG00, Bit 0 (EXREF) in the SPI. In the 28-lead TSSOP package, the reference can be disabled by raising REFLO to AVDD. In both packages, the reference can also be overridden by an external reference with no effect on performance. REFIO serves as either an input or an output depending on whether the internal or an external reference is used. Table 13 summarizes the reference operation for the LFCSP and TSSOP package options.

Reference Mode	REFIO pin	LFCSP	TSSOP
Internal	Connect 0.1 µF Capacitor	REG00, Bit 0 = 0 (default)	REFLO = ACOM
External	Apply External Reference	REG00, Bit 0 = 1	REFLO = AVDD

Table 13. Reference Operation (TSSOP and LFCSP packages)

To use the internal reference, simply decouple the REFIO pin to ACOM with a 0.1 µF capacitor and enable the internal reference. To enable the internal reference in the 28-lead TSSOP package, connect REFLO to ACOM via a resistance less than 5Ω. In the LFCSP package, a logic 0 must be written to REG00, Bit 0 in the SPI. (Note that this is the default configuration for the LFCSP package.) The internal reference voltage will be present at REFIO. If the voltage at REFIO is to be used anywhere else in the circuit, an external buffer amplifier with an input bias current of less than 100 nA should be used. An example of the use of the internal reference is shown in Figure 26.

TBD

Figure 26. Internal Reference Configuration

An external reference can be applied to REFIO, as shown in

TBD

Figure 27. The external reference may provide either a fixed reference voltage to enhance accuracy and drift performance or a varying reference voltage for gain control. Note that the 0.1 µF compensation capacitor is not required since the internal reference is overridden, and the relatively high input impedance of REFIO minimizes any loading of the external reference.

TBD

Figure 27. External Reference Configuration

REFERENCE CONTROL AMPLIFIER

The AD9707 contains a control amplifier that is used to regulate the full-scale output current, I_{OUTFS}. The control amplifier is configured as a V-I converter, as shown in Figure 26, so that its current output, I_{REF}, is determined by the ratio of the V_{REFIO} and an external resistor, R_{SET}, as stated in Equation

(4). I_{REF} is copied to the segmented current sources with the proper scale factor to set IOUTFS, as stated in Equation

(3).

The control amplifier allows a 5:1 adjustment span of I_{OUTFS} from 1 mA to 5 mA by setting I_{REF} between 31.25 µA and 156.25 µA (R_{SET} between 6.4 kΩ and 32 kΩ). The wide adjustment span of I_{OUTFS} provides several benefits. The first relates directly to the power dissipation of the AD9707, which is proportional to I_{OUTFS} (refer to the Power Dissipation section). The second benefit relates to the ability to adjust the output over a 14 dB range, which is useful for system gain control purposes.

The small signal bandwidth of the reference control amplifier is approximately 500 kHz and can be used for low frequency small signal multiplying applications.

DAC TRANSFER FUNCTION

The AD9707 provides complementary current outputs, IOUTA and IOUTB. IOUTA provides a near fullscale current output, I_{OUTFS}, when all bits are high (i.e., DAC CODE = 16383), while IOUTB, the complementary output, provides no current. The current output appearing at IOUTA and IOUTB is a function of both the input code and I_{OUTFS} and can be expressed as

$$IOUTA = (DAC\ CODE/16384) \times I_{OUTFS} \quad (1)$$

$$IOUTB = (16383 - DAC\ CODE)/16384 \times I_{OUTFS} \quad (2)$$

where DAC CODE = 0 to 16383 (i.e., decimal representation).

As mentioned previously, I_{OUTFS} is a function of the reference current I_{REF}, which is nominally set by a reference voltage, V_{REFIO}, and external resistor, R_{SET}. It can be expressed as

$$I_{OUTFS} = 32 \times I_{REF} \quad (3)$$

where

$$I_{REF} = V_{REFIO} / R_{SET} \quad (4)$$

The two current outputs will typically drive a resistive load directly or via a transformer. If dc coupling is required, IOUTA

and IOUTB should be directly connected to matching resistive loads, R_{LOAD}, that are tied to analog common, ACOM. The single-ended voltage output appearing at the IOUTA and IOUTB nodes is simply

$$V_{OUTA} = IOUTA \times R_{LOAD} \quad (5)$$

$$V_{OUTB} = IOUTB \times R_{LOAD} \quad (6)$$

Note: To achieve the maximum output compliance of 1 V at the nominal 2 mA output current, R_{LOAD} must be set to 500Ω.

Also note that the full-scale value of V_{OUTA} and V_{OUTB} should not exceed the specified output compliance range to maintain specified distortion and linearity performance

The 28-lead TSSOP package option contains two internal resistors (R_{SET} = 16 kΩ and R_{LOAD} = 500 Ω) that can be used to configure the AD9707 with a reduced number of external resistors. Connecting the RSET pin to the FSADJ pin sets the full scale output current to 2 mA without the need for an external R_{SET} resistor. Connecting the RLOAD pin to IOUTA allows the user to generate a single-ended output driving into a 500 Ω load without the need for an external R_{LOAD} resistor.

$$V_{DIFF} = (IOUTA - IOUTB) \times R_{LOAD} \quad (7)$$

Substituting the values of IOUTA, IOUTB, I_{REF}, and V_{DIFF} can be expressed as

$$V_{DIFF} = \{(2 \times DAC\ CODE - 16383)/16384\} (32 \times V_{REFIO} / R_{SET}) \times R_{LOAD} \quad (8)$$

Equations

(7) and

(8) highlight some of the advantages of operating the AD9707 differentially. First, the differential operation helps cancel common-mode error sources associated with IOUTA and IOUTB, such as noise, distortion, and dc offsets. Second, the differential code dependent current and subsequent voltage, V_{DIFF}, is twice the value of the single-ended voltage output (i.e., V_{OUTA} or V_{OUTB}), thus providing twice the signal power to the load.

Note that the gain drift temperature performance for a single-ended (V_{OUTA} and V_{OUTB}) or differential output (V_{DIFF}) of the AD9707 can be enhanced by selecting temperature tracking resistors for R_{LOAD} and R_{SET} due to their ratiometric relationship, as shown in Equation

(8).

ANALOG OUTPUTS

The complementary current outputs in each DAC, IOUTA, and IOUTB may be configured for single-ended or differential operation. IOUTA and IOUTB can be converted into complementary single-ended voltage outputs, V_{OUTA} and V_{OUTB}, via a load resistor, R_{LOAD}, as described in the DAC Transfer Function section by Equations

(5) through

(8). The differential voltage, V_{DIFF}, existing between V_{OUTA} and V_{OUTB}, can also be converted to a single-ended voltage via a transformer or differential amplifier configuration. The ac performance of the AD9707 is optimum and specified using a differential transformer-coupled output in which the voltage swing at IOUTA and IOUTB is limited to ±0.5 V.

The distortion and noise performance of the AD9707 can be enhanced when it is configured for differential operation. The common-mode error sources of both IOUTA and IOUTB can be significantly reduced by the common-mode rejection of a transformer or differential amplifier. These common-mode error sources include even-order distortion products and noise. The enhancement in distortion performance becomes more significant as the frequency content of the reconstructed waveform increases and/or its amplitude increases. This is due to the first order cancellation of various dynamic common-mode distortion mechanisms, digital feedthrough, and noise.

Performing a differential-to-single-ended conversion via a transformer also provides the ability to deliver twice the reconstructed signal power to the load (assuming no source termination). Since the output currents of IOUTA and IOUTB are complementary, they become additive when processed differentially.

As mentioned above, if the AD9707 is being used at its nominal operating point of 2 mA output current, and 1 V output swing is desired, R_{LOAD} must be set to 500Ω. A properly selected transformer will allow the AD9707 to provide the required power and voltage levels to different loads.

The output impedance of IOUTA and IOUTB is determined by the equivalent parallel combination of the PMOS switches associated with the current sources and is typically 200 MΩ in parallel with 5 pF. It is also slightly dependent on the output voltage (i.e., V_{OUTA} and V_{OUTB}) due to the nature of a PMOS device. As a result, maintaining IOUTA and/or IOUTB at a virtual ground via an I-V op amp configuration will result in the optimum dc linearity. Note that the INL/DNL specifications for the AD9707 are measured with IOUTA maintained at a virtual ground via an op amp.

IOUTA and IOUTB also have a negative and positive voltage compliance range that must be adhered to in order to achieve optimum performance. The negative output compliance range of –1 V is set by the breakdown limits of the CMOS process. Operation beyond this maximum limit may result in a

breakdown of the output stage and affect the reliability of the AD9707.

The positive output compliance range is slightly dependent on the full-scale output current, I_{OUTFS}. It degrades slightly from its nominal 1.2 V for an I_{OUTFS} = 2 mA to 1 V for an I_{OUTFS} = 1 mA. The optimum distortion performance for a single-ended or differential output is achieved when the maximum full-scale signal at IOUTA and IOUTB does not exceed 0.5 V.

ADJUSTABLE OUTPUT COMMON MODE (LFCSP ONLY)

The 32-lead LFCSP package option provides the ability to set the output common mode to a value other than ACOM via pin 19 (OTCM). This option allows the user to directly interface the output of the AD9707 to components that require common mode levels other than 0 V. The OTCM pin contains some amount of data switching current and thus should be actively driven to the desired voltage level when not tied directly to ACOM. Optium performance is achieved when the voltage on OTCM is equal to the center of the output swing on IOUTA and IOUTB.

Note that setting OTCM to a voltage greater than ACOM allows the peak of the output signal to be closer to the positive supply rail. To prevent distortion in the output signal due to limited available headroom, the supply voltage, common mode level must be chosen such that the following expression is satisfied:

$$A_{VDD} - V_{OTCM} > 2.0V \quad (10)$$

DIGITAL INPUTS

The AD9707 digital section consists of 14 input bit channels and a clock input. The 14-bit parallel data inputs can follow standard positive binary or twos complement coding, where DB13 is the most significant bit (MSB) and DB0 is the least significant bit (LSB). IOUTA produces a full-scale output current when all data bits are at Logic 1. IOUTB produces a complementary output with the full-scale current split between the two outputs as a function of the input code.

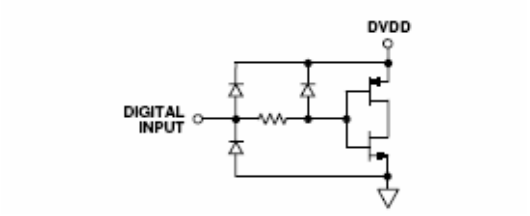


Figure 28. Equivalent Digital Input

The digital interface is implemented using an edge-triggered master/slave latch. The DAC output updates on the rising edge of the clock and is designed to support a clock rate as high as 175 MSPS. The clock can be operated at any duty cycle that meets the specified latch pulsewidth. The setup and hold times can also be varied within the clock cycle as long as the specified minimum times are met, although the location of these transition edges may affect digital feedthrough and distortion performance. Best performance is typically achieved when the input data transitions on the falling edge of a 50% duty cycle clock.

CLOCK INPUT

TSSOP Package

The 28-lead TSSOP package option has a single-ended clock input (CLOCK) that must be driven to rail-to-rail CMOS levels. The quality of the DAC output is directly related to the clock quality and jitter is a key concern. Any noise or jitter in the clock will translate directly into the DAC output. Optimal performance will be achieved if the CLOCK input has a sharp rising edge, since the DAC latches are positive edge triggered.

LFCSP Package

A configurable clock input is available in the 32-lead LFCSP package, which allows for a single-ended and a differential clock mode. The mode selection can be controlled either by the CMODE pin if the SPI is disabled or through SPI REG02, Bit 2 (CLKDIFF) if the SPI is enabled. Connecting CMODE to CLKCOM selects the single-ended clock input. In this mode, the CLK+ input is driven with rail-to-rail swings and the CLK– input is left floating. If CMODE is connected to CLKVDD, the differential receiver mode is selected. In this mode, both inputs are high impedance. Table 14 summarizes the clock mode control for the LFCSP version of the AD9707. There is no significant performance difference between the clock input modes.

SPI Disabled CMODE Pin	SPI Enabled REG02, Bit 2	Clock Input Mode
CLKCOM	0	Single-Ended
CLKVDD	1	Differential

Table 14. Clock Mode Selection (LFCSP package)

The single-ended clock in the LFCSP package has the same operating requirements as the TSSOP single-ended clock. Please refer to the section describing the TSSOP single-ended clock input for details on operating requirements.

In the differential input mode, the clock input functions as a high impedance differential pair. The common-mode level of the CLK+ and CLK– inputs can vary from 0.75 V to 2.25 V, and the differential voltage can be as low as 0.5 V p-p. This mode can be used to drive the clock with a differential sine wave since the high gain bandwidth of the differential inputs will convert the sine wave into a single-ended square wave internally.

DAC TIMING

Input Clock and Data Timing Relationship

Dynamic performance in a DAC is dependent on the relationship between the position of the clock edges and the time at which the input data changes. The AD9707 is rising-

edge triggered, and so exhibits dynamic performance sensitivity when the data transition is close to this edge. In general, the goal when applying the AD9707 is to make the data transition close to the falling clock edge. This becomes more important as the sample rate increases. Figure 29 shows the relationship of SFDR to clock placement with different sample rates. Note that at the lower sample rates, more tolerance is allowed in clock placement, while at higher rates, more care must be taken.

TBD

Figure 29. SFDR vs. Clock Placement @ f_{OUT}=20 MHz and 50 MHz

POWER DISSIPATION

The power dissipation, P_D, of the AD9707 is dependent on several factors that include:

- The power supply voltages (AVDD, CVDD, and DVDD)
- The full-scale current output I_{OUTFS}
- The update rate f_{CLOCK}
- The reconstructed digital input waveform

The power dissipation is directly proportional to the analog supply current, I_{AVDD}, and the digital supply current, I_{DVDD}. I_{AVDD} is directly proportional to I_{OUTFS}, as shown in Figure 30, and is insensitive to f_{CLOCK}. Conversely, I_{DVDD} is dependent on both the digital input waveform, f_{CLOCK}, and digital supply DVDD. Figure 31 shows I_{DVDD} as a function of full-scale sine wave output ratios (f_{OUT}/f_{CLOCK}) for various update rates with DVDD = 3.3 V. I_{CLKVDD} is directly proportional to f_{CLOCK}, and is higher for differential clock operation than single-ended operation. This difference in clock current is due primarily to the differential clock receiver which is disabled in single-ended clock mode.

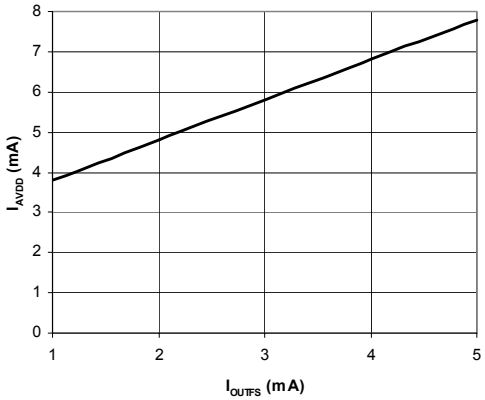


Figure 30. I_{AVDD} vs I_{OUTFS}

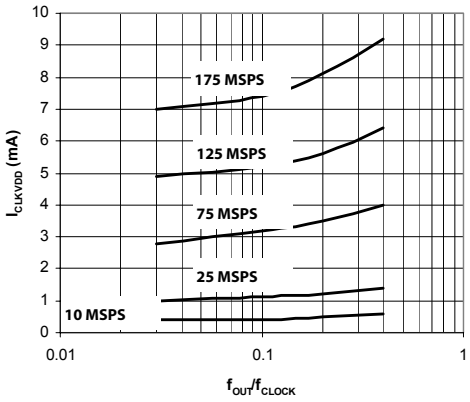


Figure 31. I_{DVDD} vs f_{OUT}/f_{CLK}Ratio @ DVDD=3.3 V

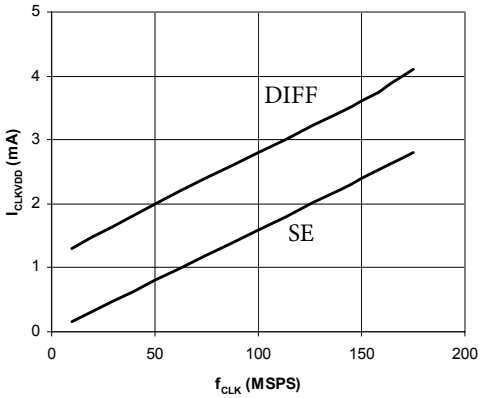


Figure 32. I_{CLKVDD} vs. f_{CLOCK} (Differential Clock Mode)

Sleep and Power-Down Mode Operation

The AD9707 has a sleep mode that turns off the output current and reduces the total supply current to less than 3.5 mA over the specified supply range of 1.7 V to 3.6 V and temperature range. This mode can be activated by applying a logic level 1 to the SLEEP pin. The SLEEP pin logic threshold is equal to 0.5Ω x AVDD. This digital input also contains an active pulldown circuit that ensures that the AD9707 remains enabled if this input is left disconnected.

The AD9707 takes less than 50 ns to power down and approximately 5 µs to power back up.

LFCSP Package

The 32-lead LFCSP package option offers three power-down functions that can be controlled through the SPI, if enabled. These power-down modes reduce the power dissipation to as little as 120 µA. The power-down functions are controlled through SPI REG00, Bits 1–3. Table 15 below summarizes the power-down functions of the AD9707 that can be controlled through the SPI. The power-down mode can be enabled by writing a logic level 1 to the corresponding bit in Register 00.

Power Down Mode	Bit (REG00)	Functional Description
Clock Off	1	Turn off clock
Sleep	2	Turn off output current

Power Down	3	Turn off clock, output current and internal voltage reference

Table 15. Power-Down Mode Selection (LFCSP package)

EVALUATION BOARD

GENERAL DESCRIPTION

The TxDAC family evaluation boards allow for easy setup and testing of any TxDAC product in the TSSOP and LFCSP packages. Careful attention to layout and circuit design, combined with a prototyping area, allows the user to evaluate the AD9707 easily and effectively in any application where low power, high resolution, high speed conversion is required.

This board allows the user the flexibility to operate the AD9707 in various configurations. Possible output configurations include transformer coupled, resistor terminated, and single and differential outputs. The digital inputs are designed to be driven from various word generators, with the on-board option to add a resistor network for proper load termination. Provisions are also made to operate the AD9707 with either the internal or external reference or to exercise the power-down feature.

OUTLINE DIMENSIONS

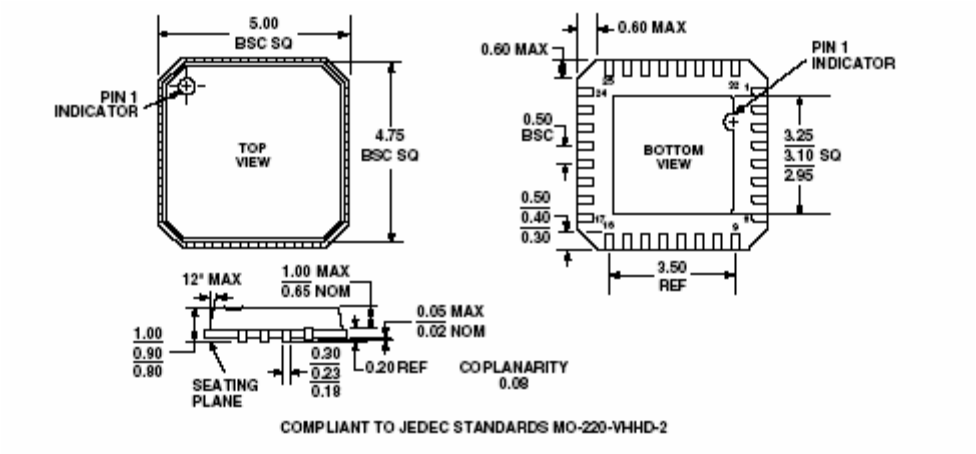


Figure 33. 32-Lead Lead Frame Chip Scale Package [LFCSP] (CP-32)
Dimensions shown in millimeters

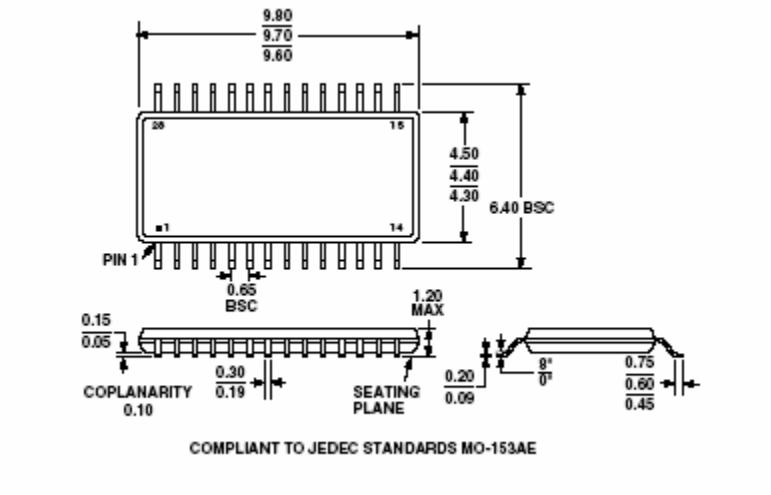


Figure 34. 28-Lead Thin Shrink Small Outline Package [TSSOP] (RU-28)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options [1]
AD9707ARUZ	-40°C to +85°C	28-Lead TSSOP	RUZ-28
AD9707ARUZRL7	-40°C to +85°C	28-Lead TSSOP	RUZ-28
AD9707ACPZ	-40°C to +85°C	32-Lead LFCSP	CPZ-32
AD9707ACPZRL7	-40°C to +85°C	32-Lead LFCSP	CPZ-32
AD9707ACP-PCB		Evaluation Board (LFCSP)	
AD9707ARU-PCB		Evaluation Board (TSSOP)	

[1] RUZ = Pb-Free Thin Shrink Small Outline Package (TSSOP); CPZ = Pb-Free Lead Frame Chip Scale Package (LFCSP)

REVISION HISTORY

Location	Page
7/05—Data Sheet changed from REV. A to REV. PrB.	
	UNIVERSAL
4/05—Data Sheet changed from REV. 0 to REV. A.	
Added 28-Lead TSSOP Package	UNIVERSAL

PR05674-0-7/05(PrB)